a plurality of data wirings formed on the substrate substantially orthogonal to the gate wirings;

a thin film transistor formed in each of the pixel areas and structured planar type having an operating semiconductor layer formed on the substrate, a gate insulating film formed on the operating semiconductor layer, a gate electrode formed on the gate insulating film and connected to one of the gate wirings, first and second semiconductor layers formed on both sides of the operating semiconductor layer electrically connected to the pixel electrode via a contact window opened to first and second insulating layers laminated on the first semiconductor layer, and a drain electrode including the second semiconductor layer and connected to the data wirings; and

a plurality of storage capacitor electrodes using the first semiconductor layer as a first storage capacitor electrode, having a second storage capacitor electrode being formed between the first insulating film and the second insulating film and connected to a storage capacitor wiring maintained at a predetermined potential, wherein at least a first storage capacitor is structured by the first storage capacitor electrode, the first insulating film and the second storage capacitor electrode, and a second storage capacitor is structured by the second storage capacitor electrode, the second insulating film and the pixel electrode.

11. (New) An active matrix type display as set forth in claim 10, wherein the first storage capacitor electrode uses a semiconductor layer formed isolated from the first semiconductor layer instead of the first semiconductor layer.

12. (New) An active matrix type display as set forth in claim 10, wherein a plurality of the storage capacitor electrodes have a third storage capacitor electrode formed on the first insulating film in the gate wiring area at a previous stage of the pixel area and connected to the pixel electrode in the pixel area, and a fourth storage capacitor electrode formed on the second insulating film in the gate wiring area and the data wiring area and providing an end of the pixel electrode formed on a third insulating film formed at an upper portion and an end overlapping viewing the substrate perpendicularly, wherein a third storage capacitor is structured by the third storage capacitor electrode, the second insulating film and the fourth storage capacitor electrode, and the fourth storage capacitor is structured by the fourth storage capacity electrode, the third insulating film and the pixel electrode.

13. (New) An active matrix type display as set forth in claim 12, wherein a fifth storage capacitor is structured by the third storage capacitor electrode, the first insulating film and the gate wiring.

14. (New) An active matrix type display as set forth in claim 12, wherein the fourth storage capacitor electrode also serves as a storage capacitor wiring.

15. (New) An active matrix type display as set forth in claim 12, wherein the fourth storage capacitor electrode also serves as a shading film.